REMARKS

Claim 1-8 are pending in this application. Claims 1-8 have been rejected. Claims 4-8 have been objected to. Claim 1 and claims 3-8 have been amended. Claim 2 has not been amended. No claims have been canceled.

Claim Objections

The examiner has objected to claims 4 - 8 for informalities. Claims 4 - 8 have been amended in accordance with the examiner's requirements. Reconsideration and withdrawal of the objections are respectfully requested.

Claim Rejections under 35 USC § 102 - Gamal

The Examiner rejected Claims 1-8 under 35 U.S.C. 102(b) as being anticipated by Gamal et al. (U.S. Pat. No. 5,754,826) (hereinafter "Gamal").

Claim 1 has been amended. The amendment to claim 1 narrows the claim to embodiments incorporating analog circuits comprising a cascode. It is respectfully submitted that analog circuits comprising a cascode are supported by the specification as originally filed, indeed all the exemplary embodiments incorporate radio frequency analog circuits comprising a cascode as is plain by inspection of the specification and drawings. Entry into the record and consideration is respectfully requested.

The rejection of claim 1 under 35 USC § 102 is respectfully traversed on the grounds that Gamal does not teach all the limitations of claim 1 as amended. For example, claim 1 recites, in part, *"...entering data representing each transistor of the set into a computer-aided design system;..."*. It is respectfully submitted that although Gamal teaches entering circuit data he does not do so at the transistor level as so does not teach or suggest data representing *each transistor*. In fact Gamal's design approach is not aimed at the transistor level but at higher levels of abstraction such as at switch, gate or macrocell levels. Approaches such as Gamal's have great utility for essentially digital circuits, but the present invention is directed to circuits that include essential analog subsystems.

In order to clarify the invention further claim 1 has been amended to clearly call out circuits comprising the types of analog circuit typically found in radio frequency integrated circuits and requiring transistor-level design methods. Gamal actually teaches away from transistor level techniques for that type of circuit in favor of a macrocell approach.

As to claim 2, it is dependent upon claim 1 and is therefore allowable for the same reasons as claim 1.

Additionally, although Gamal and the other prior art cited by the examiner may teach the use of robust geometries for I-O transistors and I-O cells they do not teach all the limitations of claim 2. In particular claim 2 (together with claim 1 upon which claim 2 depends) recite, in part:

> *" ... identifying a first subset of the set of transistors ...wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail ... and... identifying a second subset of the set of transistors, wherein the transistors of the second subset are input-output transistors...".* and *"...designating... robust geometries for the transistors of the first subset..."* and *"...designating... robust geometries for the transistors of the second subset..."*

The above limitations make it plain that in claim 2, transistors other than I-O transistors are designated for robust geometries. This designation of non-I-O transistors facilitates achieving appropriate scaling to achieve some of the aims of the invention. In any case these limitations are not taught or suggested by Gamal.

As to claims 3 and 8, the examiner repeats essentially the same argument as for claim 1. Claims 3 and 8 have been amended in essentially the same way as claim 1. Entry into the record and consideration is requested. Moreover, it is respectfully suggested that claims 3 and 8 are allowable under 35 USC § 102 for essentially the same reasons as claim 1 as above.

As to claims 4-7, these are dependent on claim 3 and are therefore allowable for the same reasons as claim 3.

Moreover, as to claim 5, it is respectfully submitted that Gamal does not teach or suggest all the limitations of claim 5 for example *"... a radio frequency circuit..."*, indeed Gamal is silent as to RF circuits.

For the reasons cited above it is respectfully submitted that claims 1-8 are allowable over Gamal.

Claim R jections under 35 USC § 102 - Dangelo

The Examiner rejected Claims 1-8 under 35 U.S.C. 102(b) as being anticipated by Dangelo et al. (U.S. Pat. No. 5,598,344) (hereinafter "Dangelo"). Essentially, as a piece of prior art with respect to the present invention, Dangelo suffers substantially the same deficiencies as Gamal described above...

Briefly, Dangelo also addresses digital techniques and hence teaches entering data at the higher levels of abstraction rather than the transistor level; and Dangelo is silent as to cascodes and indeed as to radio frequency circuits in general.

For the reasons cited above it is respectfully submitted that claims 1-8 are allowable over Dangelo.

Claim Rejections under 35 USC § 102 in general

For the reasons recited above it is respectfully submitted that claims 1-8 are allowable under 35 USC § 102 and reconsideration and allowance under 35 USC § 102 is requested.

Conclusions

For these reasons, it is submitted that all pending claims are now in condition for allowance and allowance thereof is requested. If the Examiner believes it would be useful to progress examination, the Examiner is respectfully requested to call agent of record N.R.H.Black at 650 726 3841.

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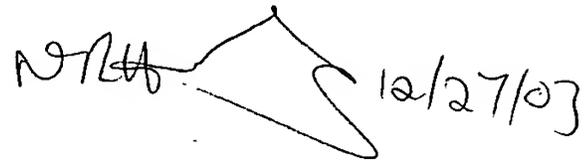
Respectfully submitted,



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